<u>CLAIMS</u>

What is claimed is:

1   1. A method, including:

2   selecting a memory access group size of about 2^N memory banks responsive

3   to receiving an indication of a change in a protocol type, wherein the group is

4   selected from a number B of banks, wherein N is associated with the protocol

5   type, and wherein N is selected so that 2^N is less than or equal to about B so that

6   a plurality of logical addresses associated with the 2^N memory banks is mapped

7   to a plurality of physical addresses associated with the number B of banks.

1   2. The method of claim 1, wherein the protocol type includes at least a first

2   operation type different from a second operation type.

1   3. The method of claim 2, wherein the first operation type includes a single-

2   instruction multiple-data operation type, and wherein the second operation

3   type includes a multiple-instruction multiple-data operation type.

1   4. The method of claim 1, further including:

2   selecting a first group size for a first data processing unit different than a

3   second group size selected for a second data processing unit, wherein the first

4   data processing unit and the second data processing unit are capable of

5   addressing the number B of banks.

1   5. The method of claim 1, wherein the indication of a protocol type is selected

2   from one of a hardware indication and a software indication.

1   6. The method of claim 1, wherein the memory access group size is associated

2   with a selected number of access bits.

1   7.   The method of claim 1, further including:

2   configuring a crossbar to operate using the memory access group size

3   responsive to receiving the indication of the change in the protocol type.

1   8. An article including a machine-accessible medium having associated

2   information, wherein the information, when accessed, results in a machine

3   performing:

4   selecting a memory access group size of about 2^N memory banks responsive

5   to receiving an indication of a change in a protocol type, wherein the group is

6   selected from a number B of banks, wherein N is associated with the protocol

7   type, and wherein N is selected so that 2^N is less than or equal to about B so that

8   a plurality of logical addresses associated with the 2^N memory banks is mapped

9   to a plurality of physical addresses associated with the number B of banks.

1   9.   The article of claim 8, wherein the protocol type is selected from at least one

2   of a single-instruction multiple-data operation type, a multiple-instruction

3   multiple-data operation type, and a combination of the single-instruction

4   multiple-data operation type and the multiple-instruction multiple-data operation

5   type.

1   10. The article of claim 8, wherein the information, when accessed, results in a

2   machine performing:

3   selecting a first memory access group size for a first data processing unit

4   different than a second memory access group size; and

5   selecting the second memory access group size for a second data processing

6   unit, wherein the first data processing unit and the second data processing unit

7   are capable of addressing the number B of banks.

1 11. An apparatus, including:

2   a selection module to select a memory access group size for at least one data

3 processing unit of about 2^N memory banks responsive to receiving an indication

4 of a change in a protocol type, wherein the group is selected from a number B of

5 banks, wherein N is associated with the protocol type, and wherein N is selected

6 so that 2^N is less than or equal to about B so that a plurality of logical addresses

7 associated with the 2^N memory banks is mapped to a plurality of physical

8 addresses associated with the number B of banks.

1 12. The apparatus of claim 11, further including:

2   a plurality of data processing units including the at least one data processing

3 units, wherein the plurality of data processing units is capable of addressing the

4 number B of banks.

1 13. The apparatus of claim 12, wherein the plurality of data processing units and

2 the number B of banks are included in a single processing element.

1 14. The apparatus of claim 12, wherein the memory access group size 2^N is

2 selected from a group of numbers including two raised to a positive integer

3 power, including 2, 4, ..., B.

1 15. The apparatus of claim 12, further including:

2   a hardware address generator to generate an address located in the 2^N

3 memory banks.

1 16. A system, including:

2   a selection module to select a memory access group size of about 2^N memory

3 banks responsive to receiving an indication of a change in a protocol type,

4 wherein the group is selected from a number B of banks, wherein N is

5 associated with the protocol type, and wherein N is selected so that 2^N is less

6 than or equal to about B so that a plurality of logical addresses associated with

7 the 2^N memory banks is mapped to a plurality of physical addresses associated

8 with the number B of banks;

9   a data processing unit capable of addressing the number B of banks; and

10   an omnidirectional antenna to transmit data processed by the data processing

11 unit.

1 17. The system of claim 16, further including:

2   a bus to couple the data processing unit to one of the number B of banks.

1 18. The system of claim 16, further including:

2   a memory to store a plurality of memory access group sizes indexed to a

3 corresponding plurality of protocol types.

1 19. The system of claim 16, further including:

2   a transceiver to couple a processing element including the data processing

3 unit to the omnidirectional antenna.

1 20. An apparatus, including:

2   a number B of memory banks addressable using a memory access group size

3 of about 2^N memory banks responsive to receiving an indication of a change in a

4 protocol type, wherein the group is selected from the number B of banks,

5 wherein N is associated with the protocol type and selected so that 2^N is less

6 than or equal to about B and wherein the protocol type consists of a single-

7 instruction multiple-data operation type, a multiple-instruction multiple-data

8 operation type, and a combination of the single-instruction multiple-data

9 operation type and the multiple-instruction multiple-data operation type.

1   21. The apparatus of claim 20, wherein the memory access group size is

2   reprogrammable and is selectable in software.

1   22. The apparatus of claim 20, further including:

2   a hardware element to store a plurality of output indications based on a

3   corresponding plurality of memory access group sizes and responsive to a

4   corresponding plurality of protocol type indications.

1   23. A method, including:

2   controlling a bandwidth of a memory coupled to a plurality of data

3   processing units responsive to a number of data processing units in use so that a

4   plurality of logical addresses associated with the memory is mapped to a

5   plurality of physical addresses associated with the memory.

1   24. The method of claim 23, wherein the number of data processing units in use

2   is responsive to an indication provided by an application to be executed.

1   25. The method of claim 23, wherein the bandwidth of the memory is associated

2   with a selected number of access bits provided by the plurality of data

3   processing units.

1   26. The method of claim 23, wherein controlling the bandwidth further includes:

2   controlling an address mapping function of the memory.